

IN THE DRAWINGS:

The attached sheets of drawings are replacement formal drawings. These sheets, which include FIGS. 1 through 20, replace all previous drawing sheets submitted in this application.

REMARKS

Claims 1 through 15 are currently pending in the application.

Claims 2, 3, and 10 are allowed.

This amendment is in response to the final Office Action of March 24, 2005.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on Yew et al. (U.S. Patent No. 6,049,129)

Claims 1, 4, 5, 7, 9, and 11 through 15 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yew et al. (U.S. Patent No. 6,049,129).

Applicant asserts that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant asserts that the Yew et al. reference does not and cannot anticipate the claimed invention of independent claims 1 and 15 under 35 U.S.C. § 102 because the Yew et al. reference does not identically describe, either expressly or inherently, each and every element of the claimed invention in as complete detail as contained in the claims.

Turning to the cited prior art, Yew et al. describes a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip 50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58,

lines 60-62). Yew et al. describes in drawing Fig. 4. the an integrated circuit package 34 comprising a silicon chip 50 attached to a printed circuit board 70 through the use of an adhesive layer 60 for which a die bonding film comprising a silver filled thermosetting type resin film.

Applicant asserts that the Yew et al. reference fails to identically describe the elements of the presently claimed inventions of presently amended independent claims 1 and 15 calling for “at least one piece of adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of the one piece of adhesive tape extending at least one of beyond said edge of said at least one semiconductor substrate opening a distance into said at least one semiconductor substrate opening to provide a detectable surface within said at least one semiconductor substrate opening and beyond said edge of said at least one semiconductor die a distance on said semiconductor substrate first surface to provide a detectable adhesive tape surface on said semiconductor substrate first surface”. Applicant asserts that the Yew et al. reference contains no description whatsoever regarding such claim limitations.

Applicant further asserts that the Yew et al. reference is silent regarding any such claim limitations. Therefore, the cited prior art does not and cannot anticipate the claimed invention under 35 U.S.C. § 102 regarding the invention of presently amended independent claims 1 and 15.

Therefore, Applicant asserts that presently amended independent claims 1 and 15 are allowable over the cited prior art. In addition, Applicant asserts that claims 4 through 9 and 11 through 14 are allowable at least because each depends either directly or indirectly from claim 1, which is allowable.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Yew et al. (U.S. Patent No. 6,049,129) in View of Khandros et al. (U.S. Patent No. 5,148,266)

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. (U.S. Patent No. 6,049,129) in view of Khandros et al. (U.S. Patent No. 5,148,266). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant asserts that dependent claim 6 is allowable since it depends from allowable presently amended independent claim 1.

Obviousness Rejection Based on Yew et al. (U.S. Patent No. 6,049,129) in View of Murakami et al. (U.S. Patent No. 5,612,569)

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. (U.S. Patent No. 6,049,129) in view of Murakami et al. (U.S. Patent No. 5,612,569). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant asserts that dependent claim 8 is allowable since it depends from allowable presently amended independent claim 1.

Applicant appreciates the allowance of claims 2, 3, and 10.

Applicant requests entry of this amendment for the following reasons:

The amendment is timely filed.

The amendment places the application in condition for allowance.

The amendment does not require any further search or consideration.

Applicant submits that claims 1, 4 through 9, and 11 through 15 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1, 4 through 9, and 11 through 15 and the case passed for issue.

Respectfully submitted,



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Attachments: Replacement Formal Drawings (10 sheets; 20 figures)